

700150 "02 Th5860

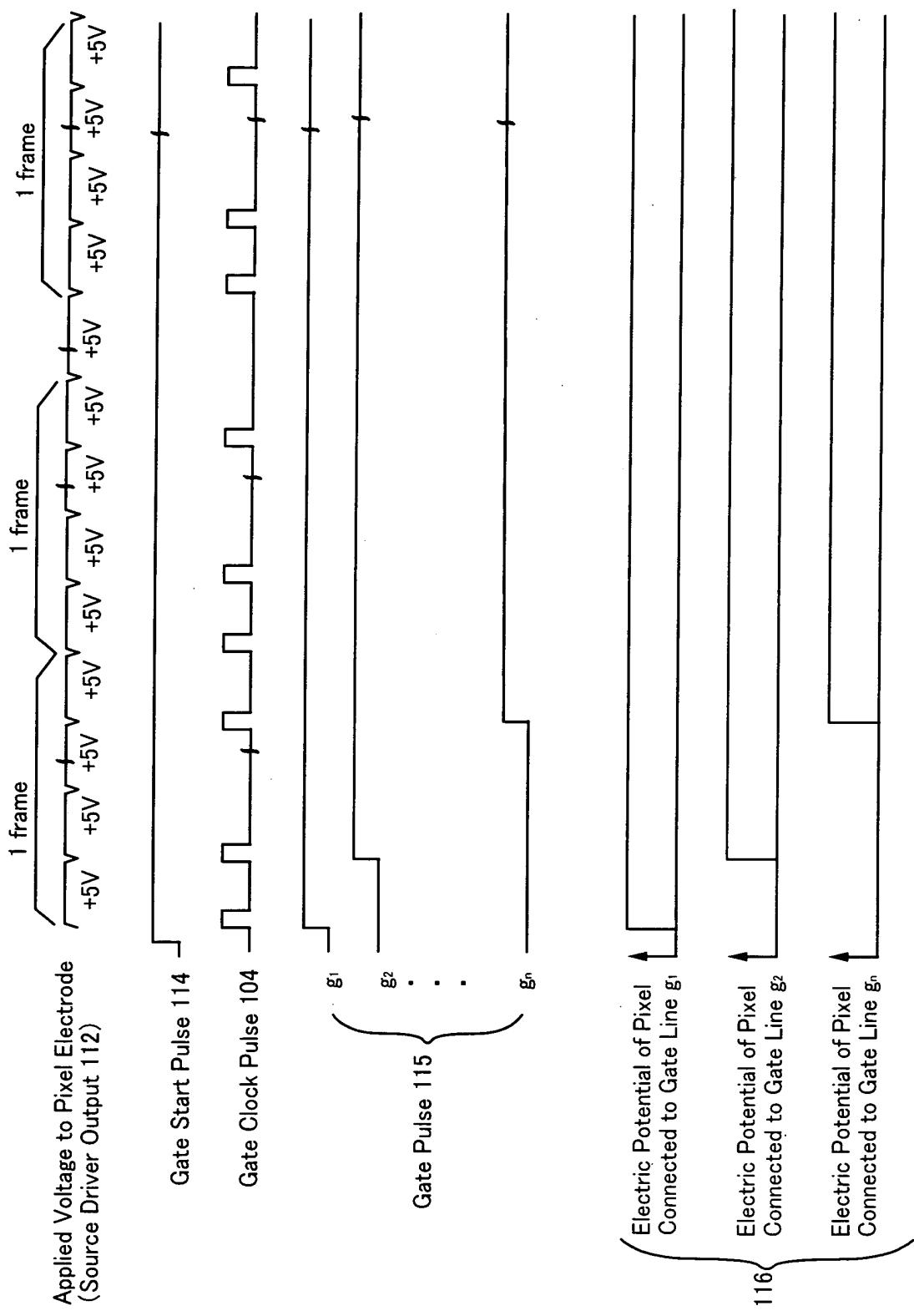


Fig. 1

“TFTS0” ପରିପ୍ରକାଶନ

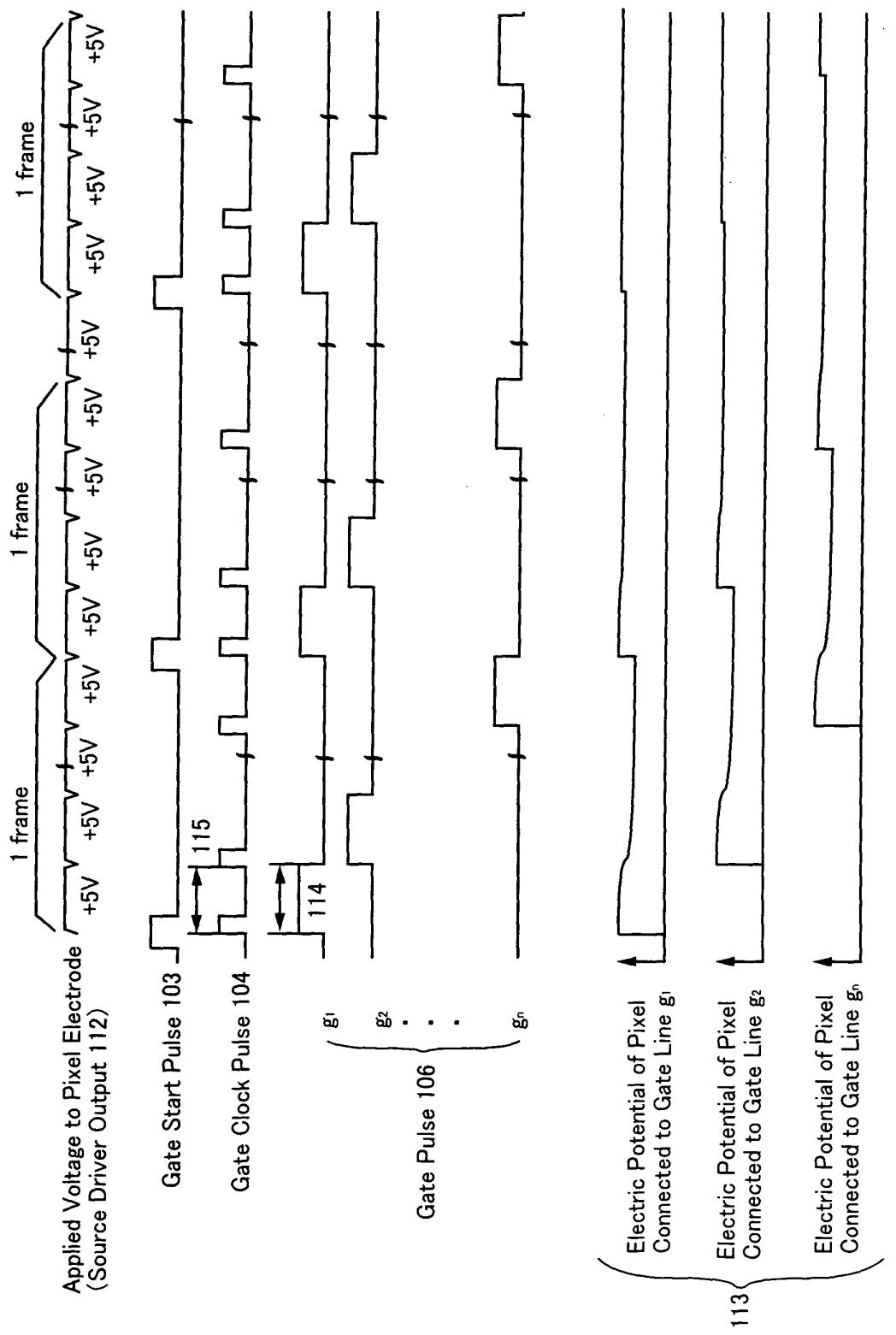


Fig. 2

T C 0 T 5 0 " 0 2 T + 5 8 6 0

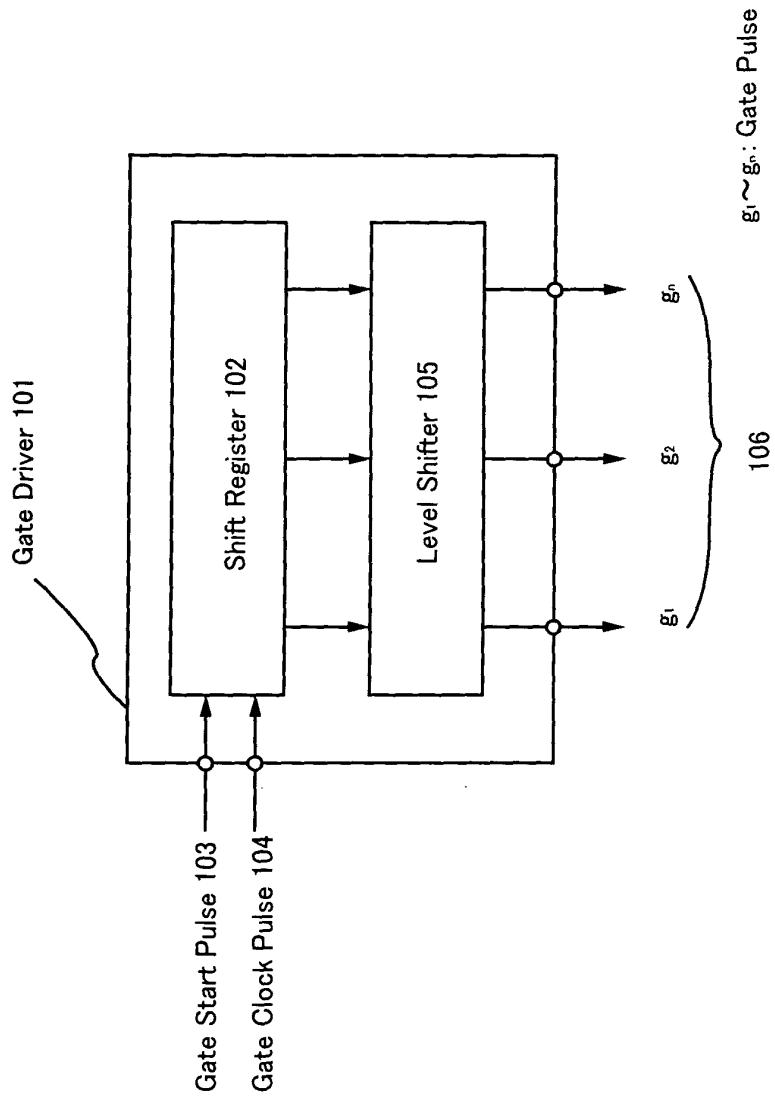


Fig. 3

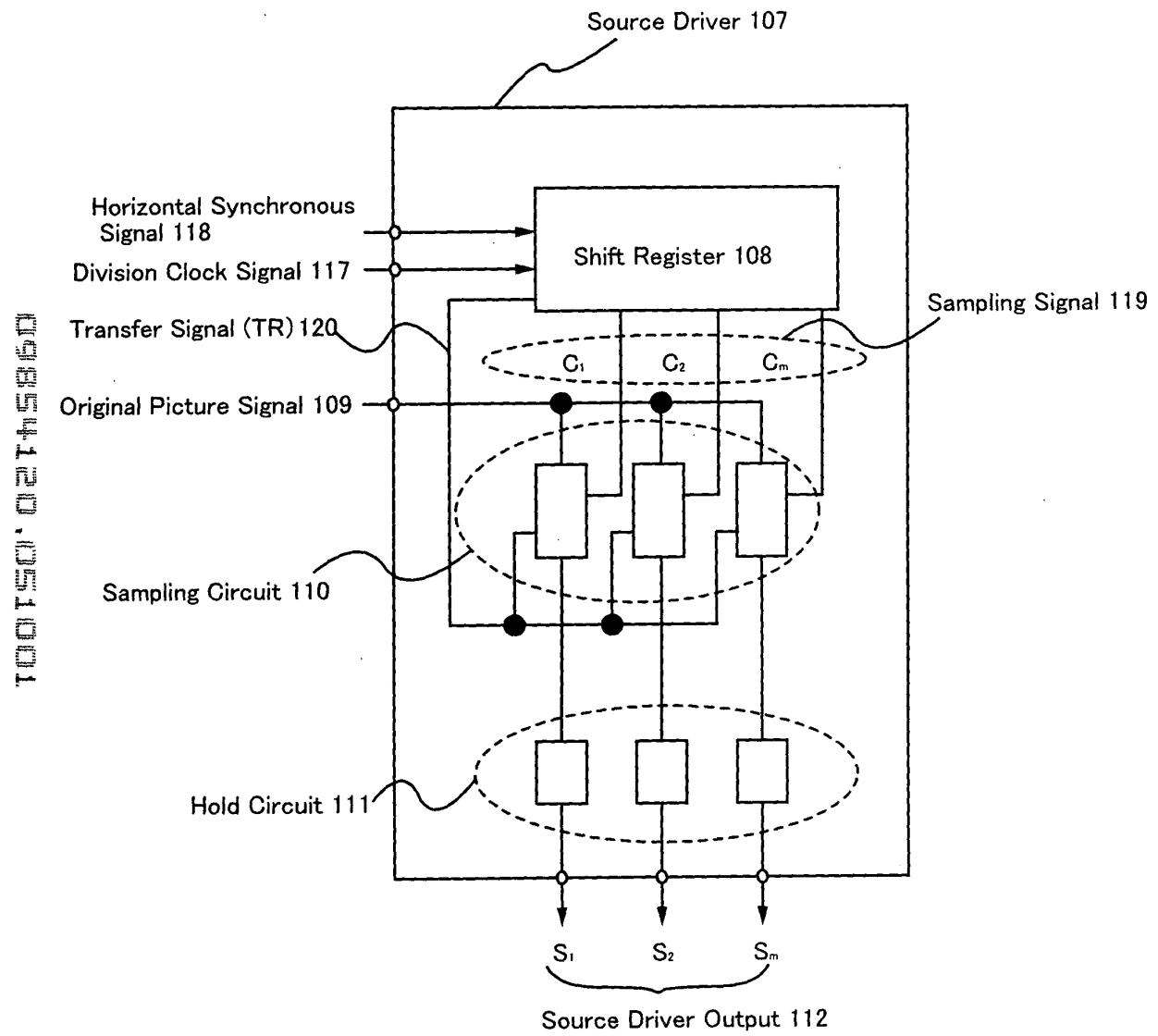


Fig. 4

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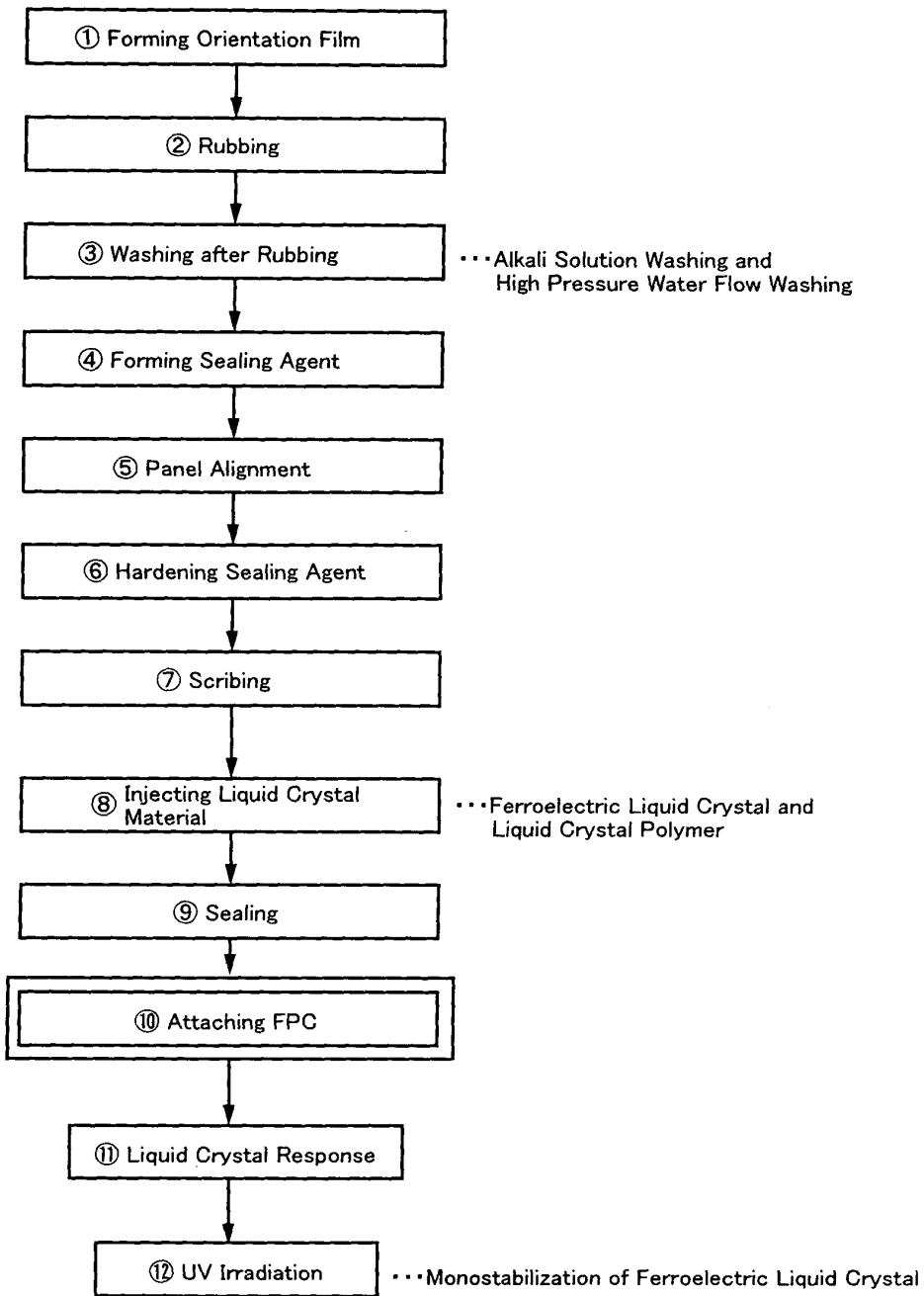
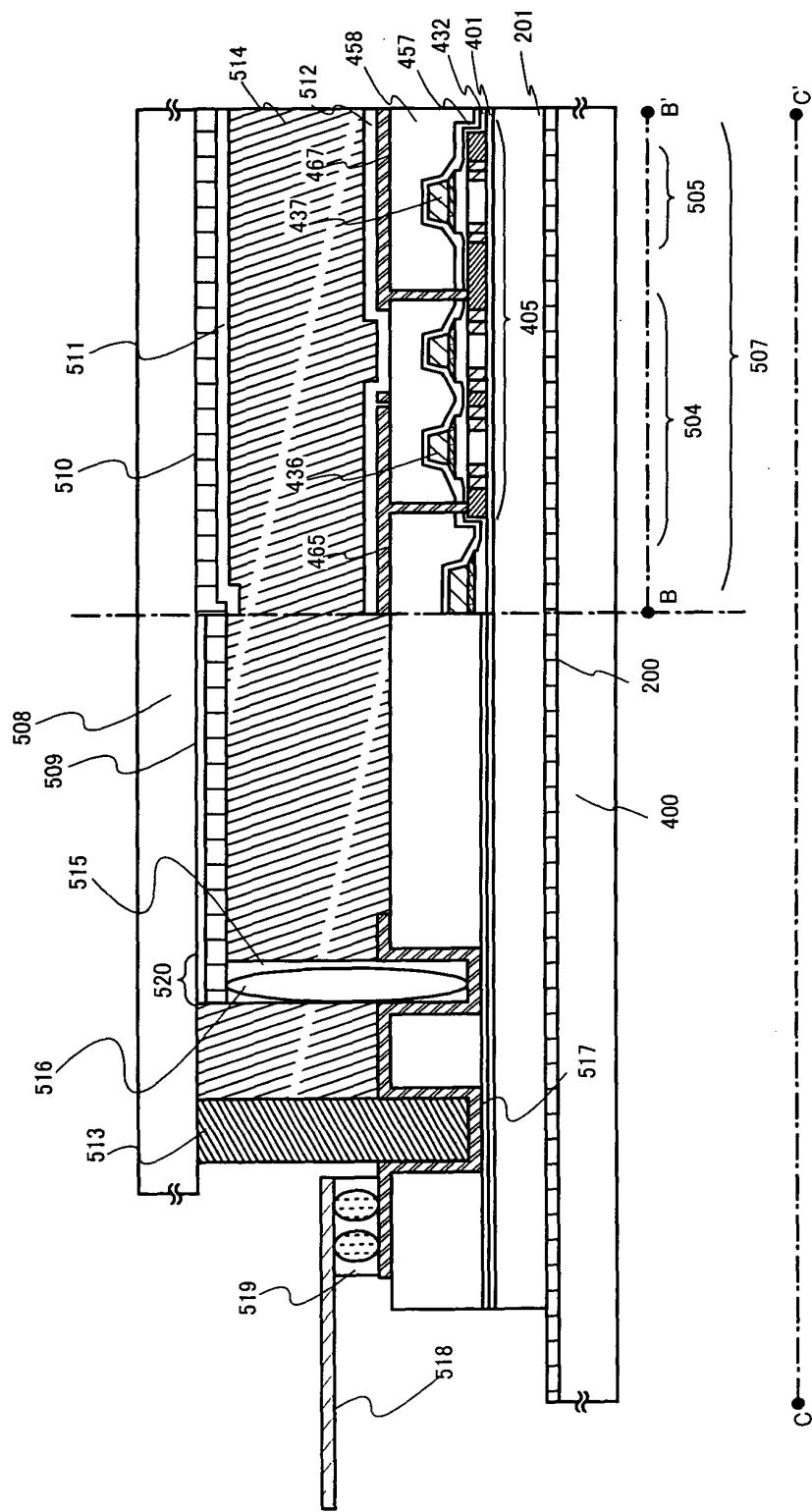


Fig. 5



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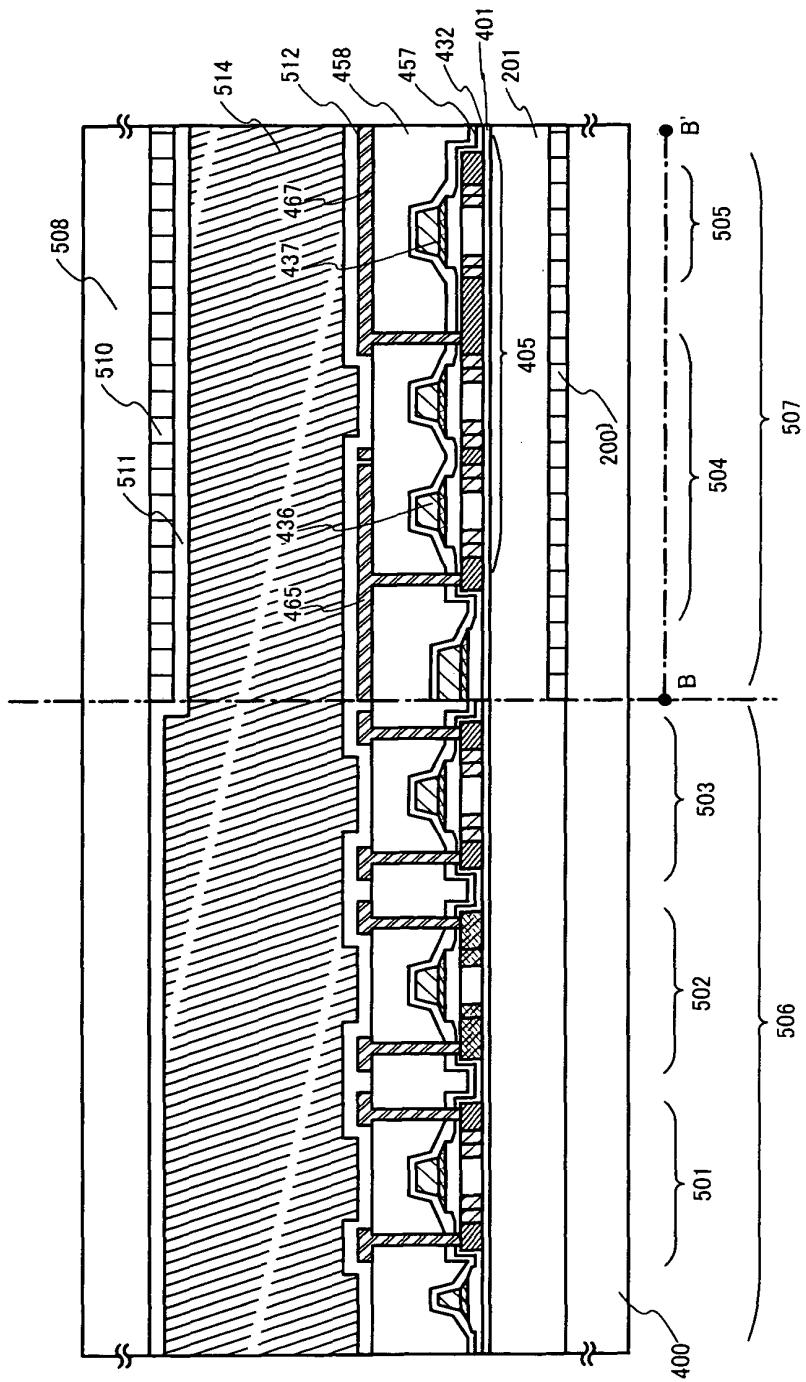


Fig. 7

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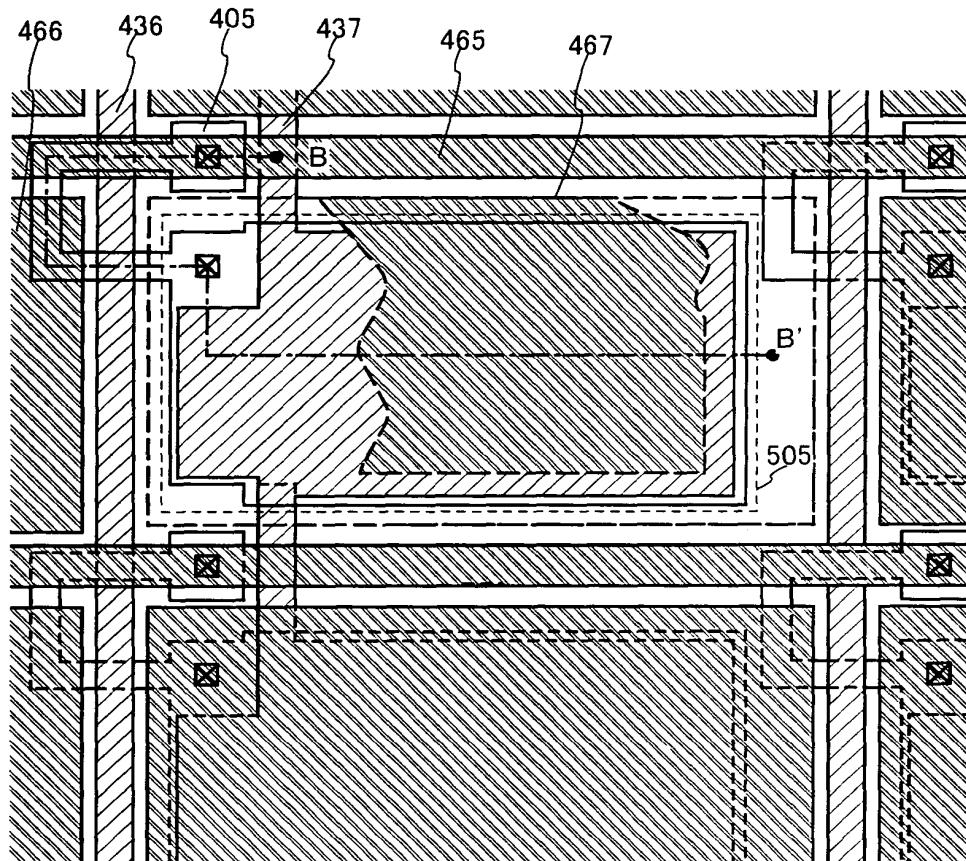


Fig. 8

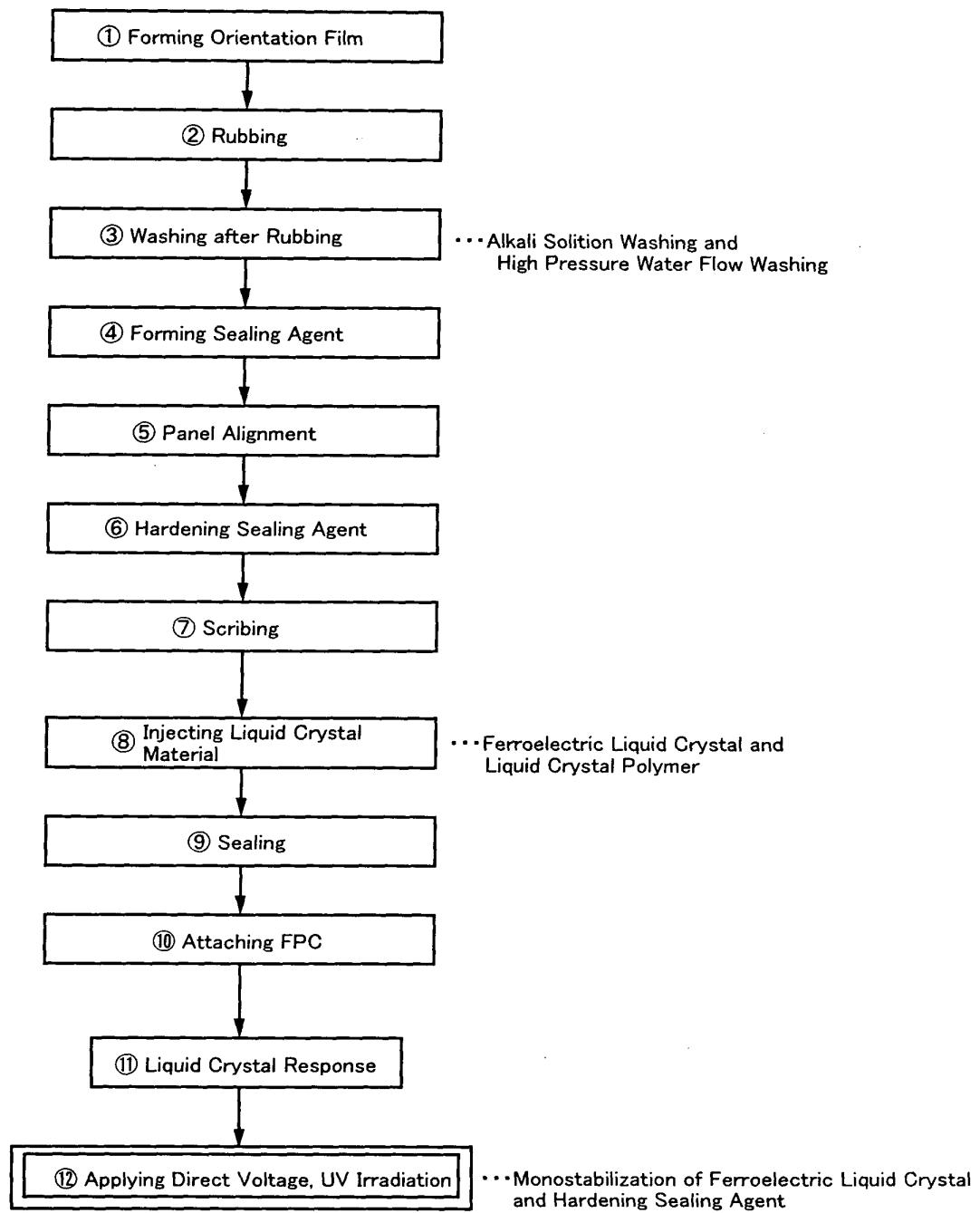


Fig. 9

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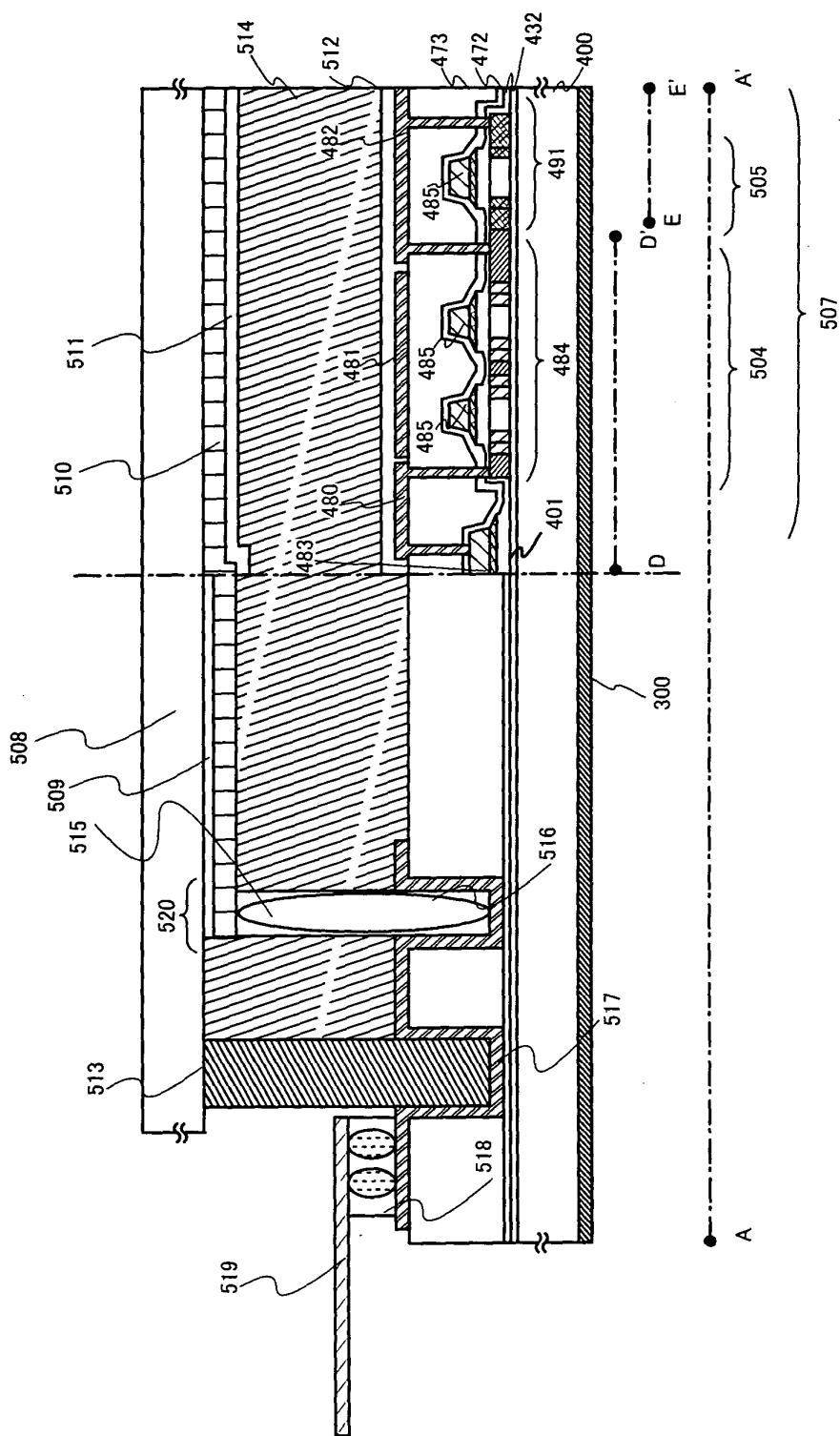
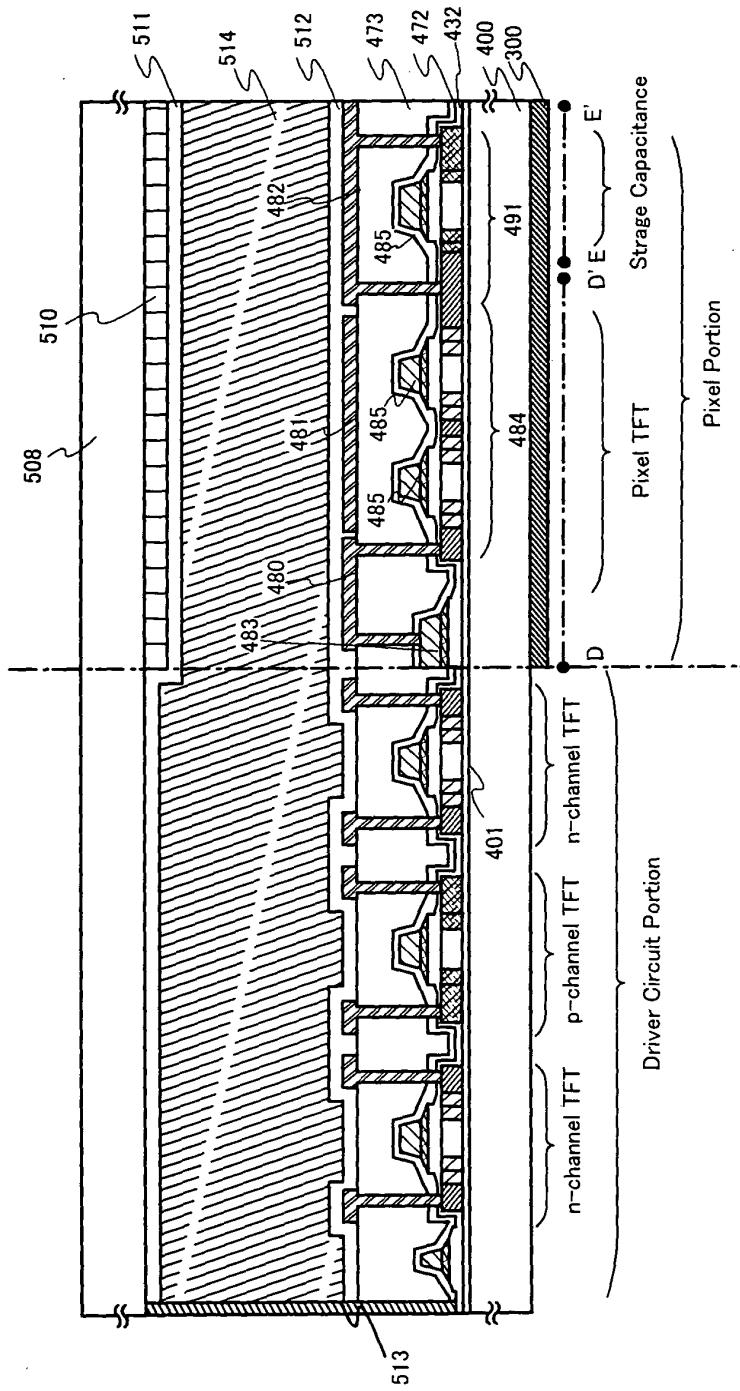


Fig. 10



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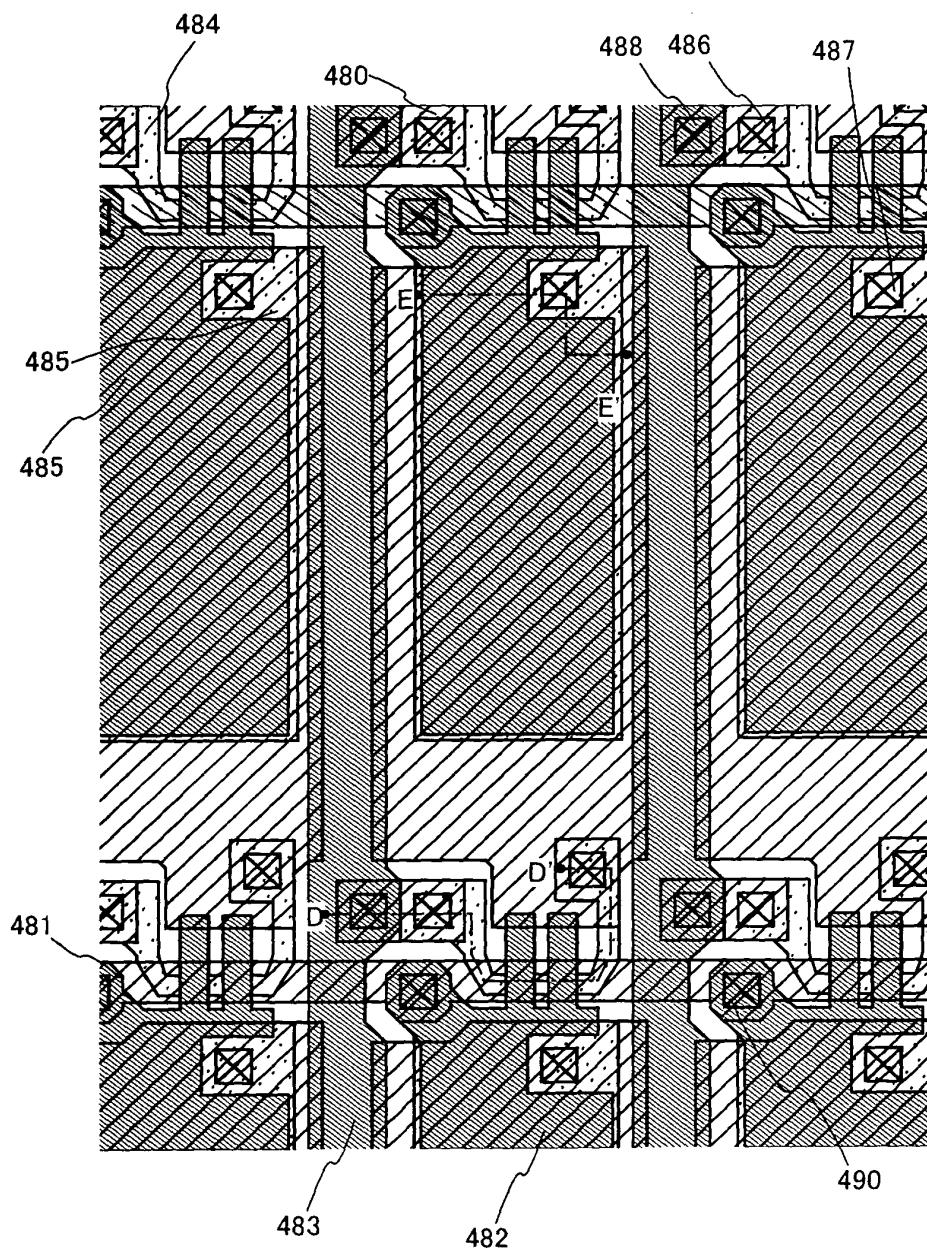


Fig. 12

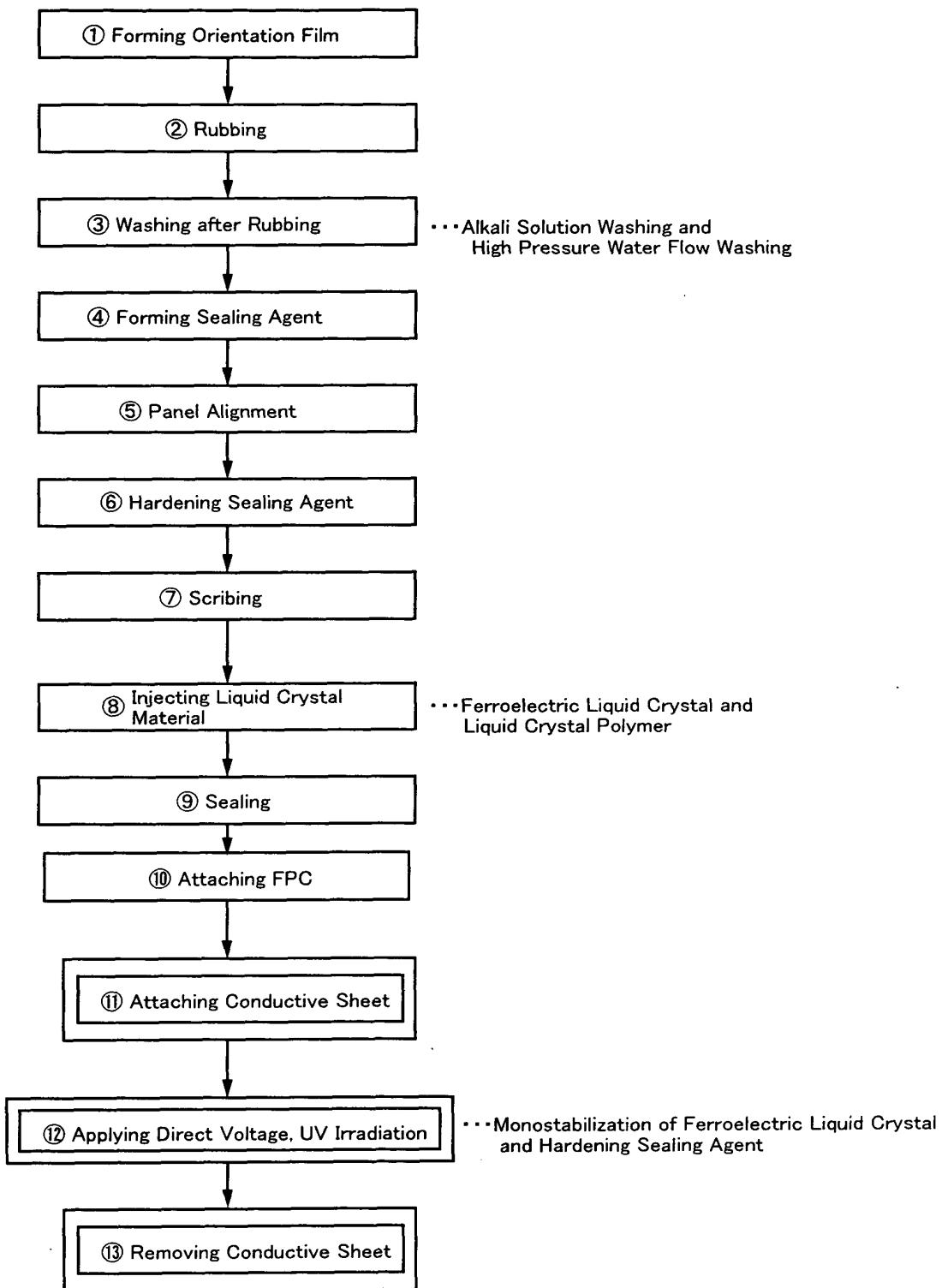


Fig. 13

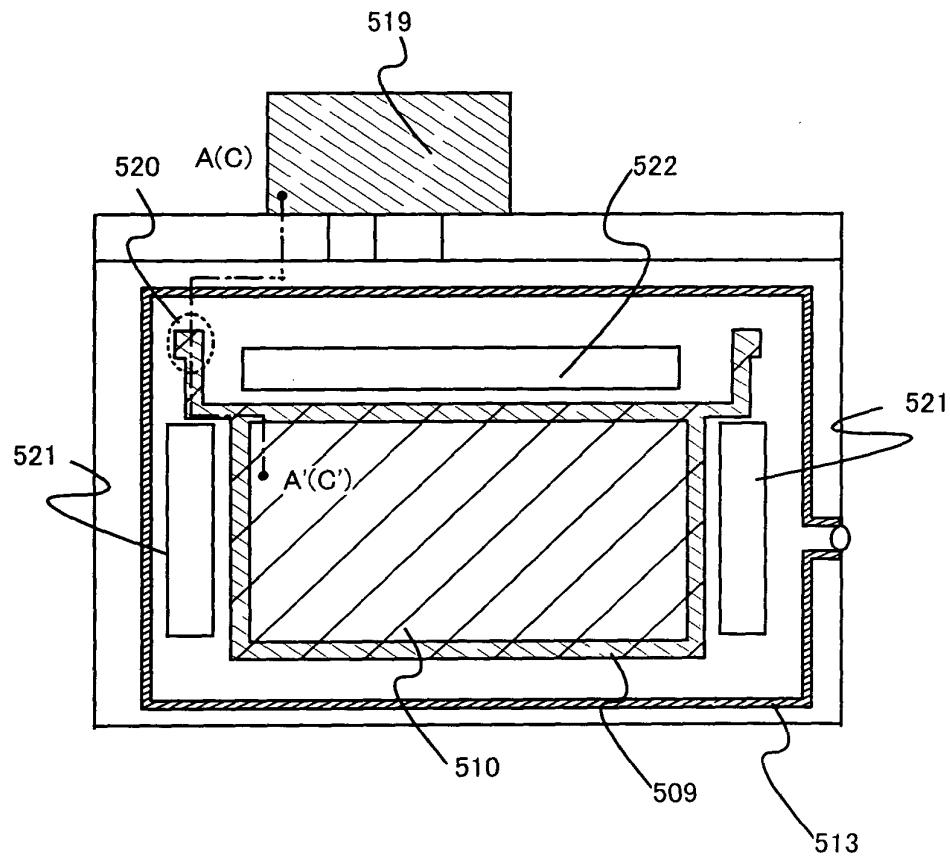
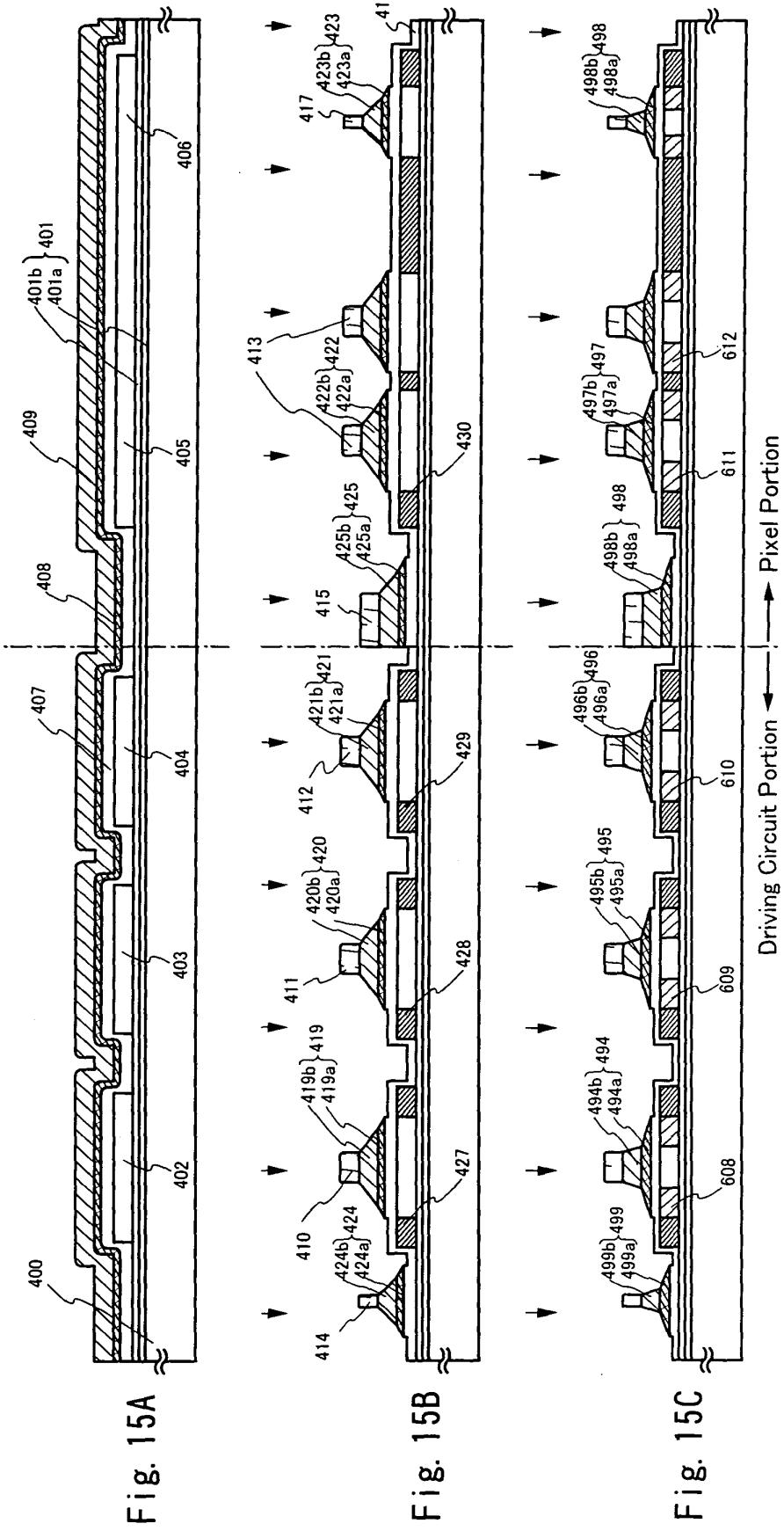


Fig. 14



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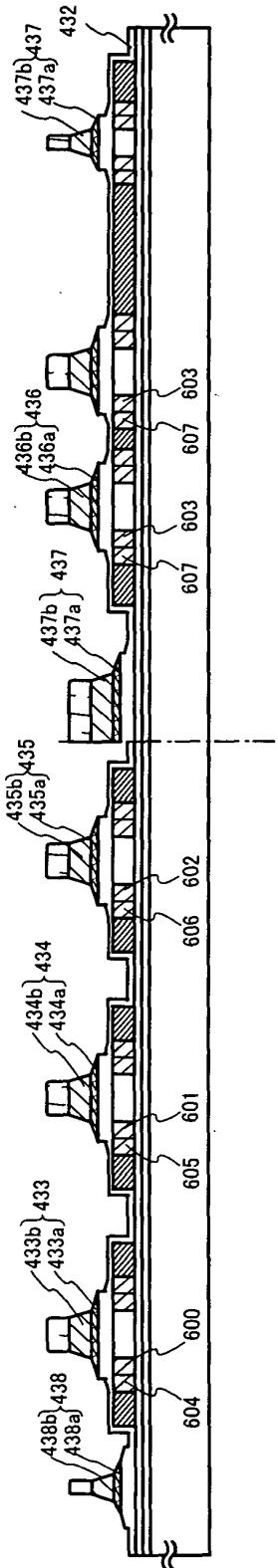


Fig. 16A

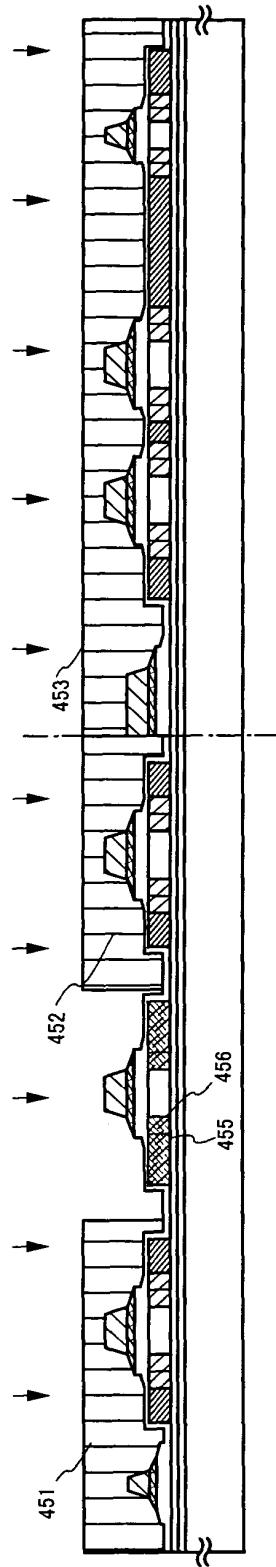


Fig. 16B

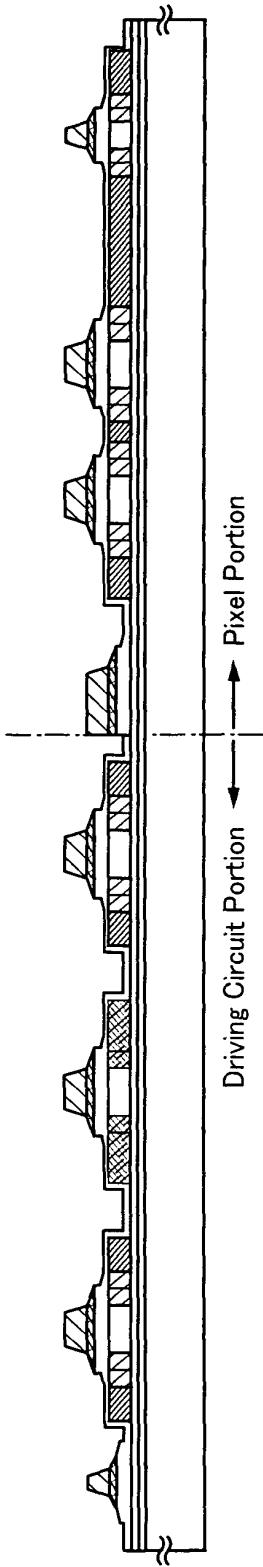


Fig. 16C

Driving Circuit Portion → Pixel Portion

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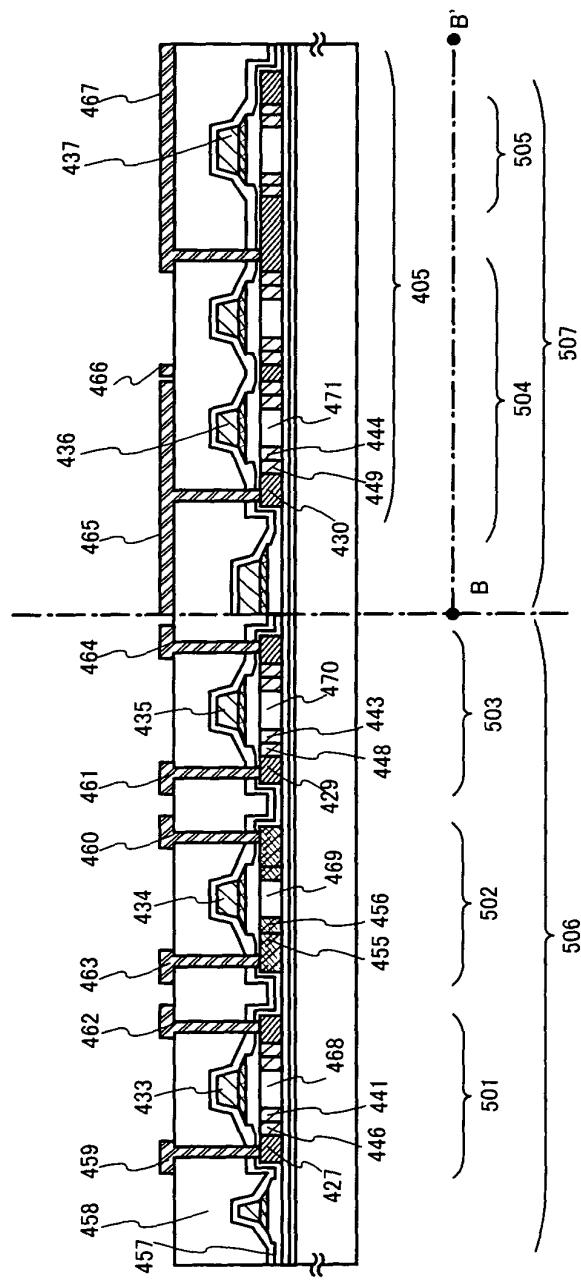


Fig. 17

FIGURE 18 "Circuit Board

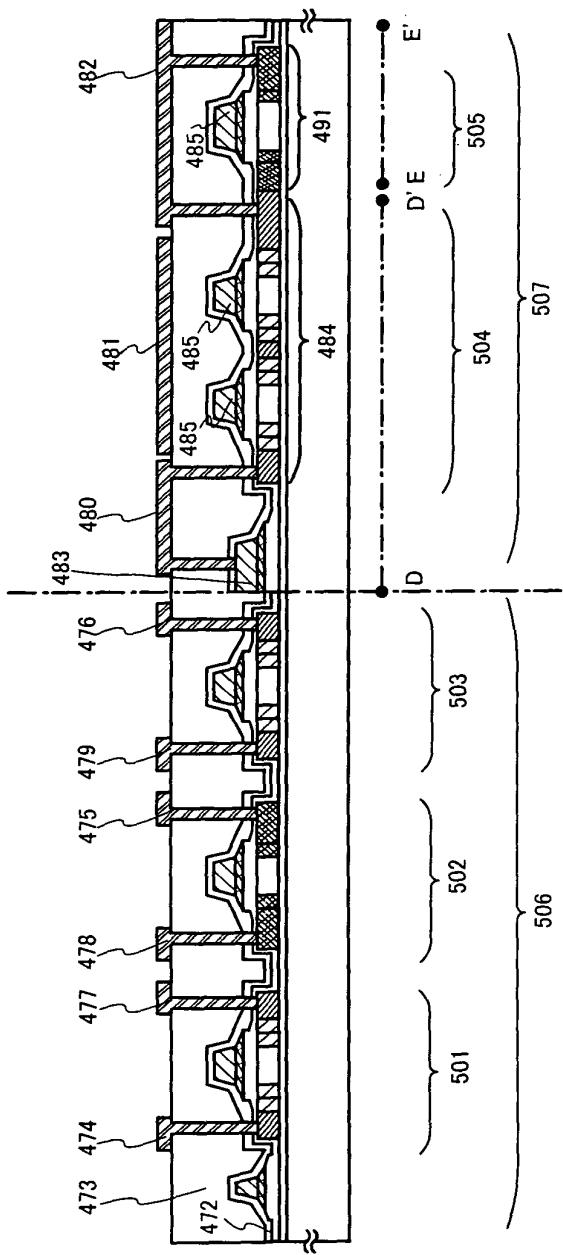


Fig. 18

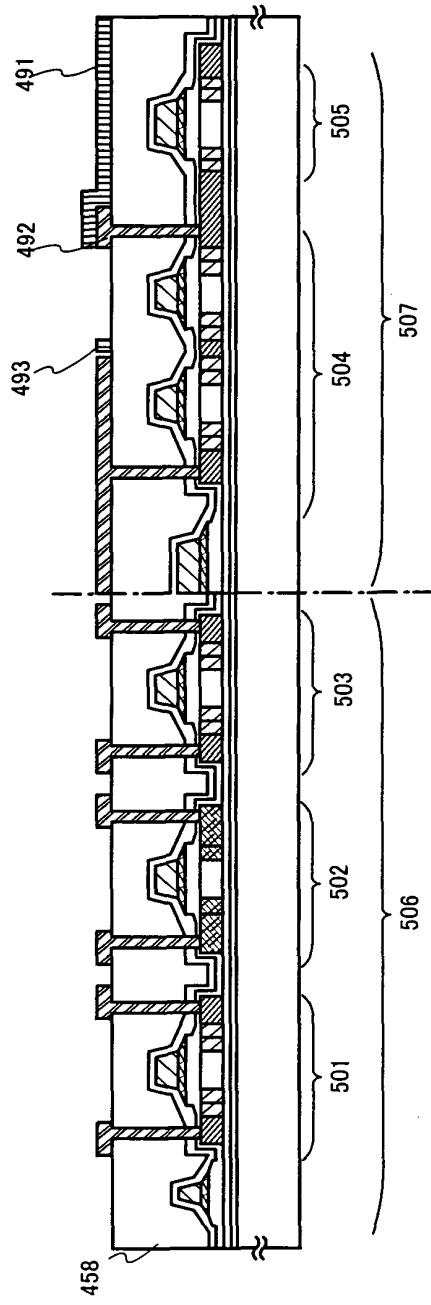


Fig. 19A

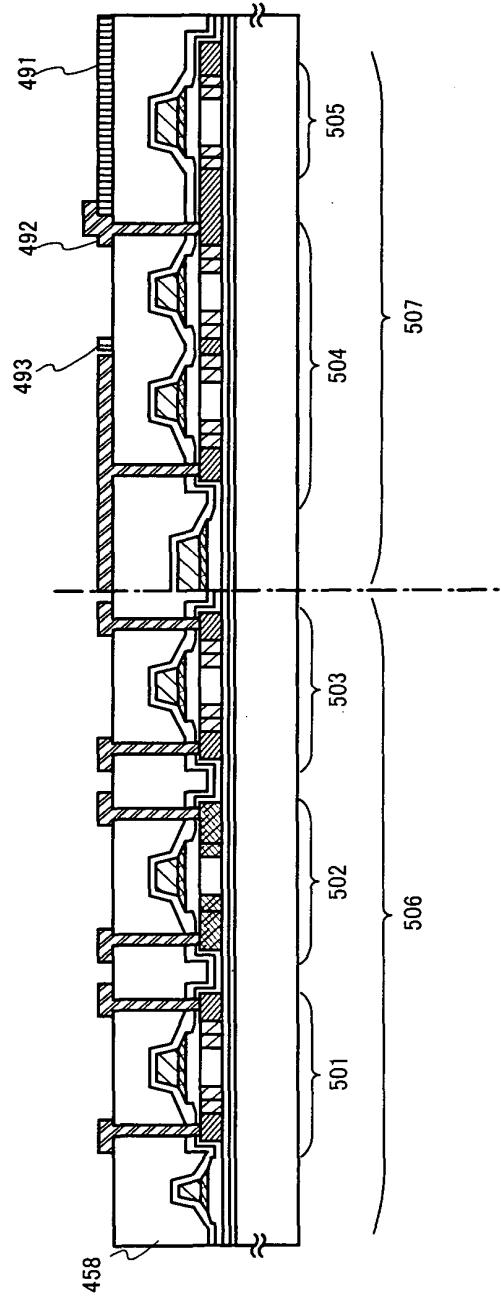


Fig. 19B

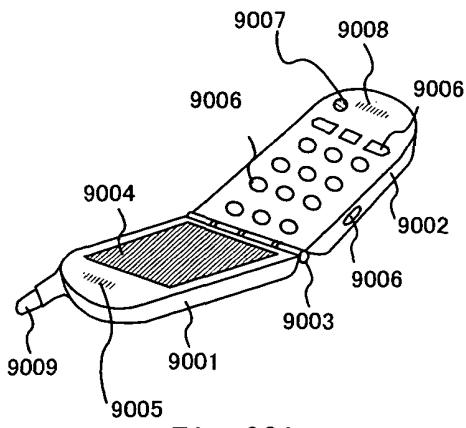


Fig. 20A

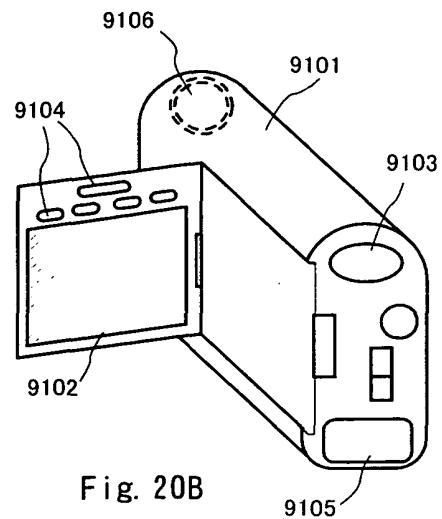


Fig. 20B

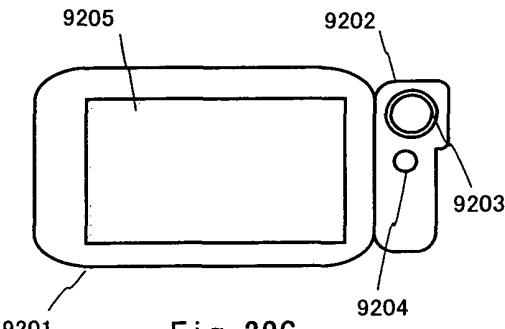


Fig. 20C

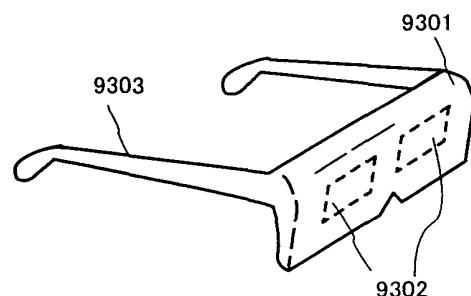


Fig. 20D

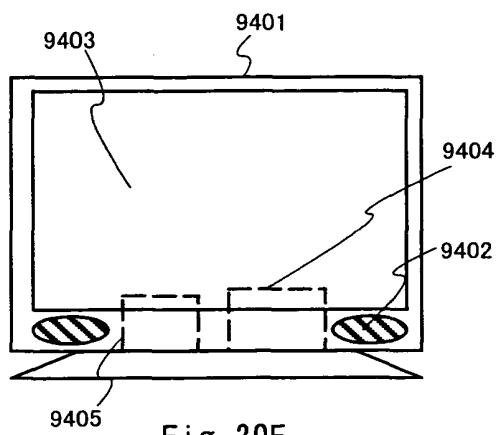


Fig. 20E

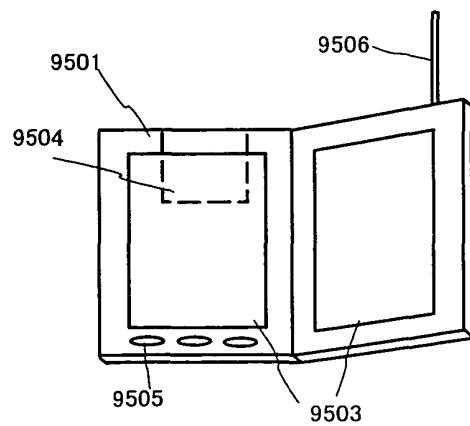


Fig. 20F

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Fig. 21A

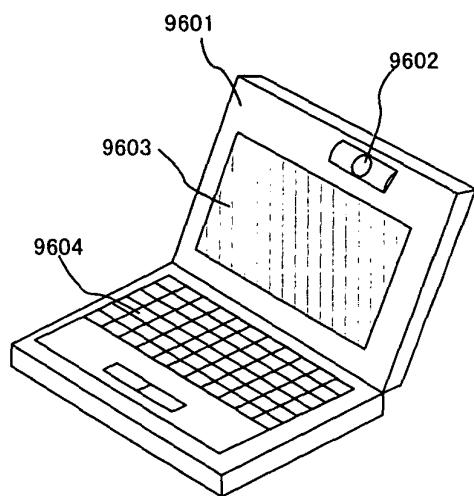


Fig. 21B

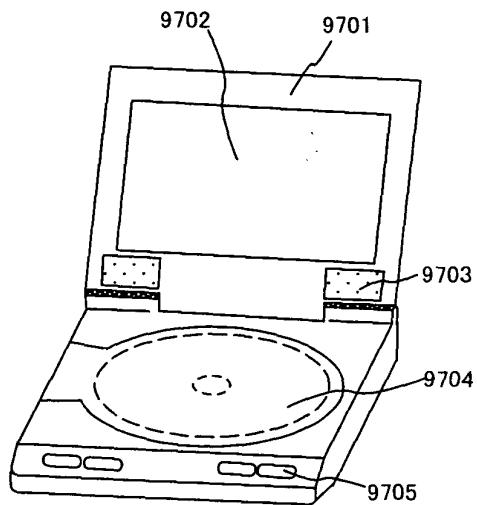
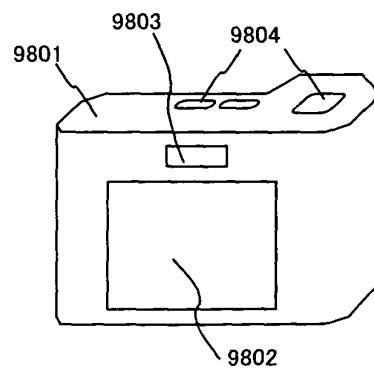


Fig. 21C



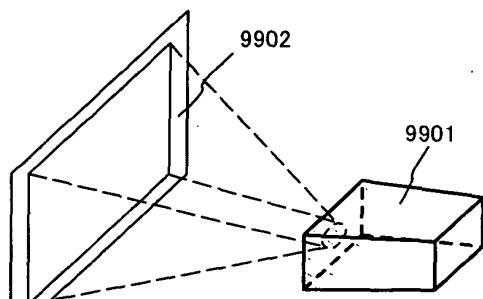


Fig. 22A

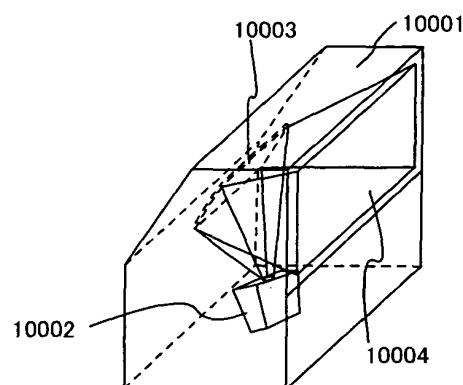


Fig. 22B

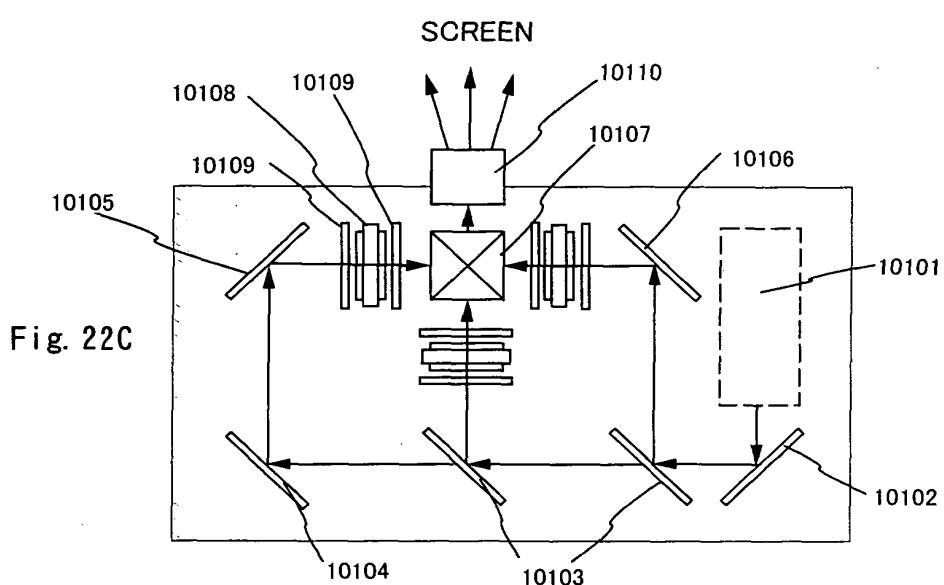


Fig. 22C

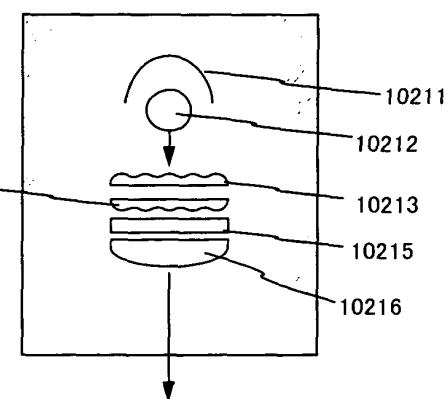


Fig. 22D

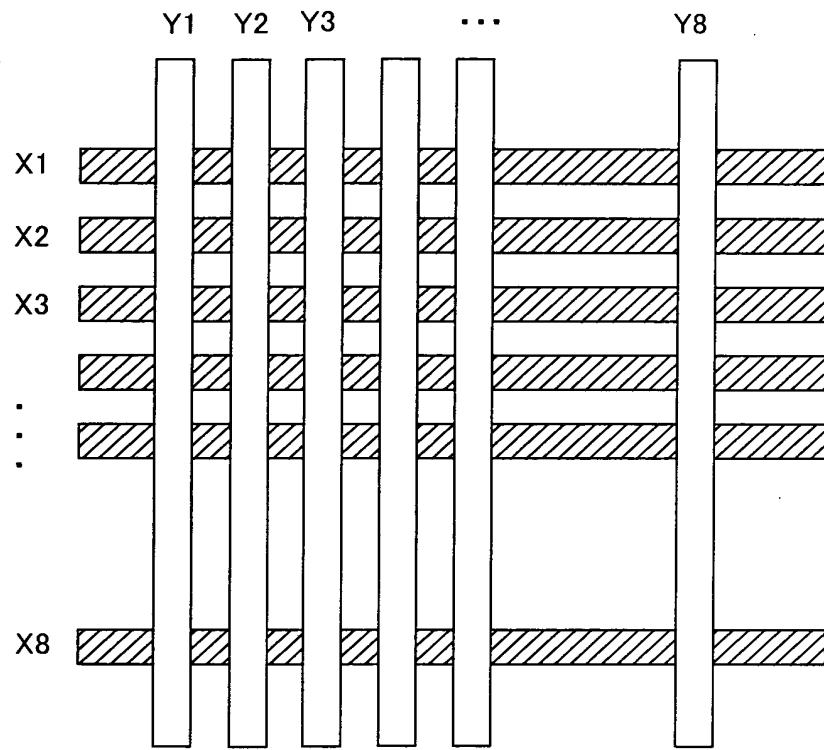


Fig. 23

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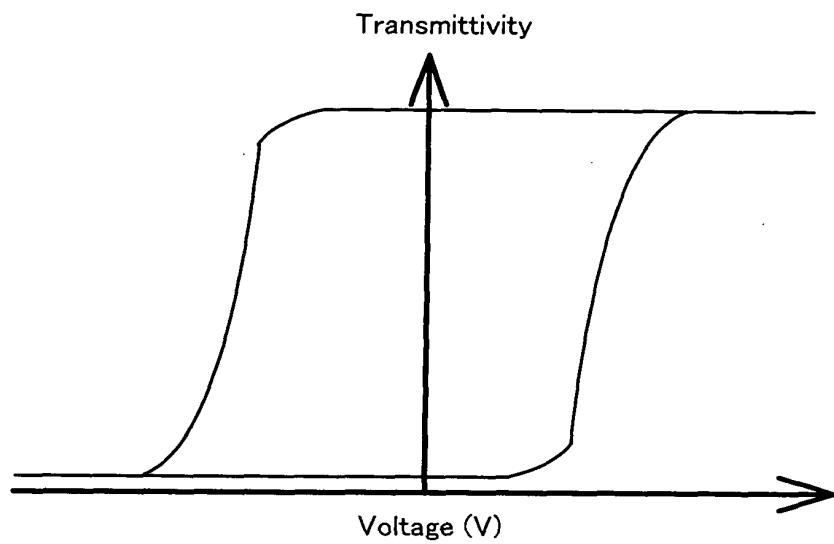


Fig. 24A

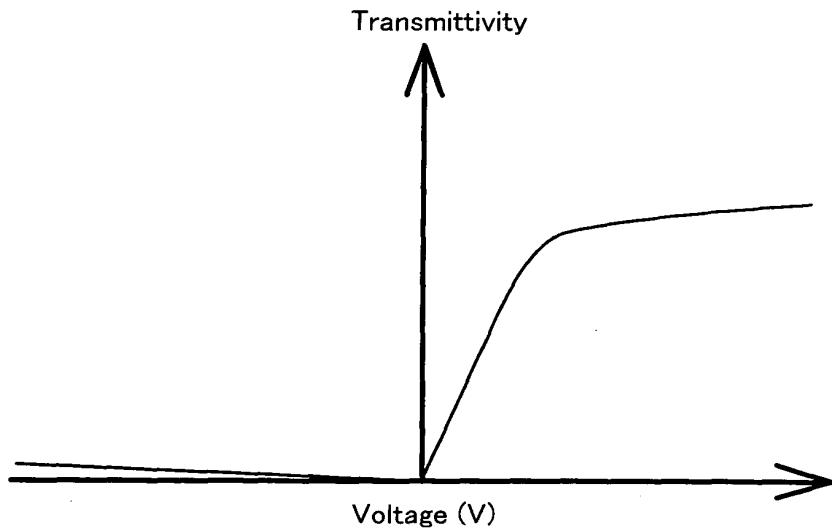


Fig. 24B

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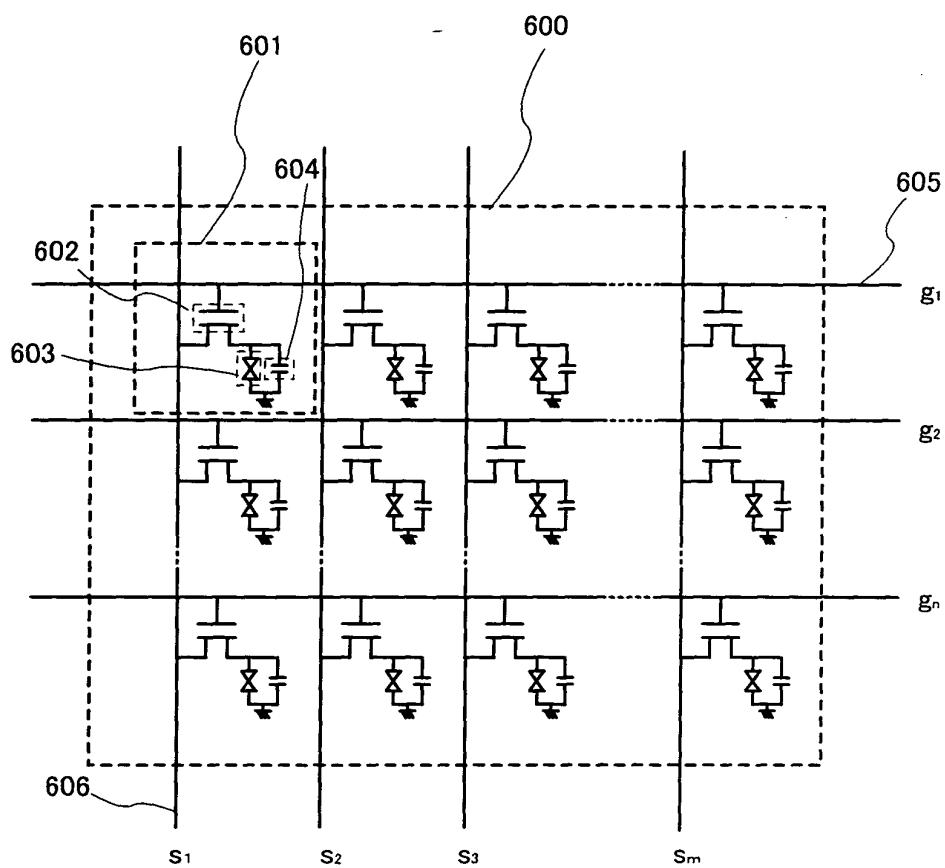


Fig. 25